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2000.039600/TT3769Serial No.  
09/853,443

List of Patents and Publications for Applicant's

Applicant  
Gulick et al.

## INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Filing Date:  
May 11, 2001Group:  
2131U.S. Patent Documents  
See Page 1Foreign Patent Documents  
See Page 1Other Art  
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## U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date of App.
	A1						
	A2						
	A3						
	A4						
	A5						

## Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						
	B2						
	B3						
	B4						
	B5						

## Other Art (Including Author, Title, Date Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
BB	C1	Intel, "Low Pin Count (LPC) Interface Specification Revision 1.0," pp. 1-31 (09/29/97)
BB	C2	Standard Microsystems Corporation, "100 Pin Enhanced Super I/O for LPC Bus with SMBus Controller for Commercial Application," Part No. LPC47B37x, pp. 1-254 (06/17/99)
BB	C3	FIPS Pub 140-1 Federal Information Processing Standards Publication, "Security Requirements for Cryptographic Modules" (01/11/1994)
BB	C4	Intel, "Communication and Networking Riser Specification," Revision 1.0 (02/07/2000)
BB	C5	"Handbook of Applied Cryptography" CRC Press 1997 pp. 154 - 157, 160 - 161, 191 - 198, 203 - 212

EXAMINER:

DATE CONSIDERED:

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